SD3931-10

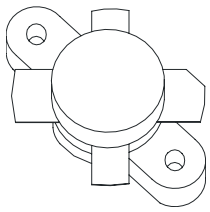
RF power transistors
HF/VHF/UHF N-channel MOSFETs

Features

- Gold metallization
- Excellent thermal stability
- Common source configuration
- P_{OUT} = 175 W min. with 23 dB gain @ 150 MHz
- In compliance with the 2002/95/EC European directive

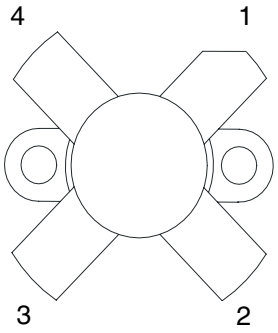
Description

The SD3931-10 is a gold metallized N-channel MOS field-effect RF power transistor. It is intended for use in 100 V DC large signal applications up to 150 MHz.



M174
Epoxy sealed

Figure 1. Pin connection



1. Drain
2. Source
3. Gate
4. Source

Table 1. Device summary

Order code	Marking	Package	Packaging
SD3931-10	SD3931-10	M174	Plastic tray

Contents

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings (T_{CASE} = 25°C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$[1]	Drain source voltage	250	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1MΩ)	250	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current	10	A
P_{DISS}	Power dissipation	389	W
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1. T_J = 150°C

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.45	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 4. Static (per side)

Symbol	Test conditions			Min	Typ	Max	Unit
$V_{(BR)DSS}$(1)	V_{GS} = 0 V	I_{DS} = 100 mA		250			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 100 V				1	mA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				250	nA
$V_{GS(Q)}$	V_{DS} = 10 V	I_D = 250 mA		1.5	2.5	4.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 5A			2.5	3.5	V
G_{FS}	V_{DS} = 10 V	I_D = 2.5 A		2.5			S
C_{ISS}	V_{GS} = 0 V	V_{DS} = 100 V	f = 1 MHz		500		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 100 V	f = 1 MHz		134		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 100 V	f = 1 MHz		6		pF

1. T_J = 150°C

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions				Min	Typ	Max	Unit
P_{1dB}	V_{DD} = 100 V	I_{DQ} = 250 mA		f = 150MHz	175	230		W
G_{PS}	V_{DD} = 100 V	I_{DQ} = 250 mA	P_{OUT} = 175W	f = 150MHz	20	21.3		dB
n_D	V_{DD} = 100 V	I_{DQ} = 250 mA	P_{OUT} = 175W	f = 150MHz	50	57		%
Load mismatch	V_{DD} = 100 V All phase angles	I_{DQ} = 250 mA	P_{OUT} = 150W	f = 150MHz	3:1			VSWR

3 Impedance data

Figure 2. Impedance data

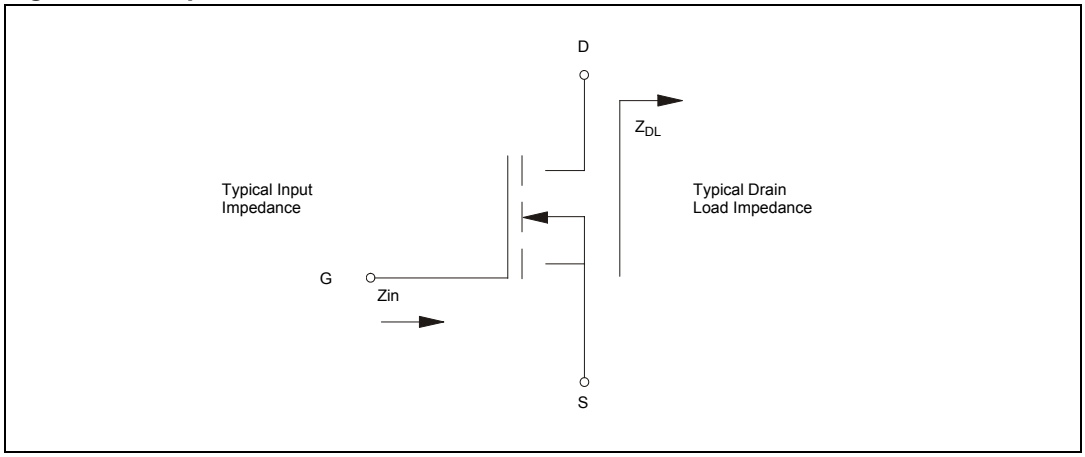


Table 6. Impedance data

Freq	Z_{IN} (Ω)	Z_{DL} (Ω)
150 MHz	0.42 - j 3.1	3.4 + j 5.5

4 Typical performance

Figure 3. Capacitances vs voltage

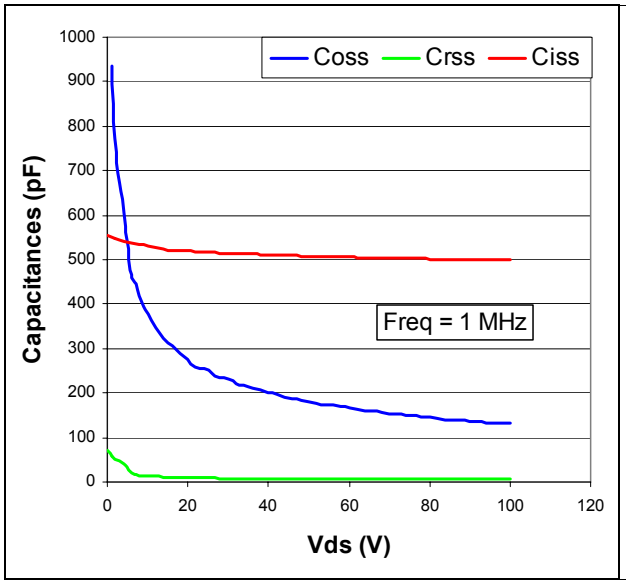


Figure 4. Gain vs output power and bias current

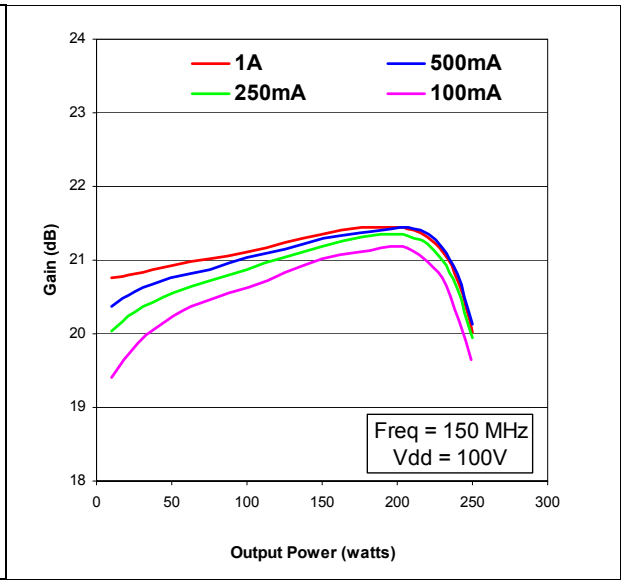


Figure 5. Output power and efficiency vs input power

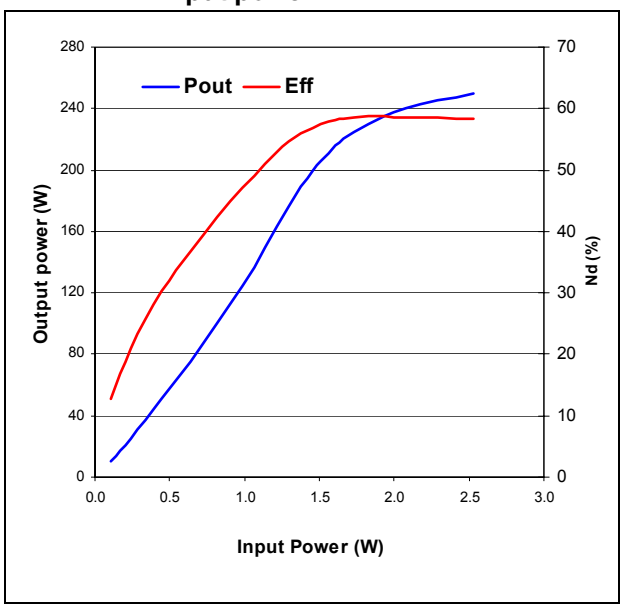


Figure 6. Zero temperature coefficient point

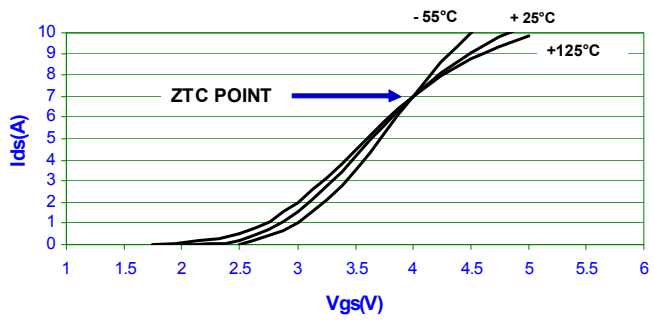


Table 7. Vgs sort (@250 mA)

Marking	Min	Max
DD	1.5	1.6
EE	1.6	1.7
FF	1.7	1.8
A	1.8	1.9
B	1.9	2
C	2	2.1
D	2.1	2.2
E	2.2	2.3
F	2.3	2.4
G	2.4	2.5
H	2.5	2.6
I	2.6	2.7
J	2.7	2.8
K	2.8	2.9
L	2.9	3
M	3	3.1
N	3.1	3.2
O	3.2	3.3
P	3.3	3.4
Q	3.4	3.5
R	3.5	3.6
S	3.6	3.7
T	3.7	3.8
U	3.8	3.9
V	3.9	4

5 Test circuit

Figure 7. Test circuit

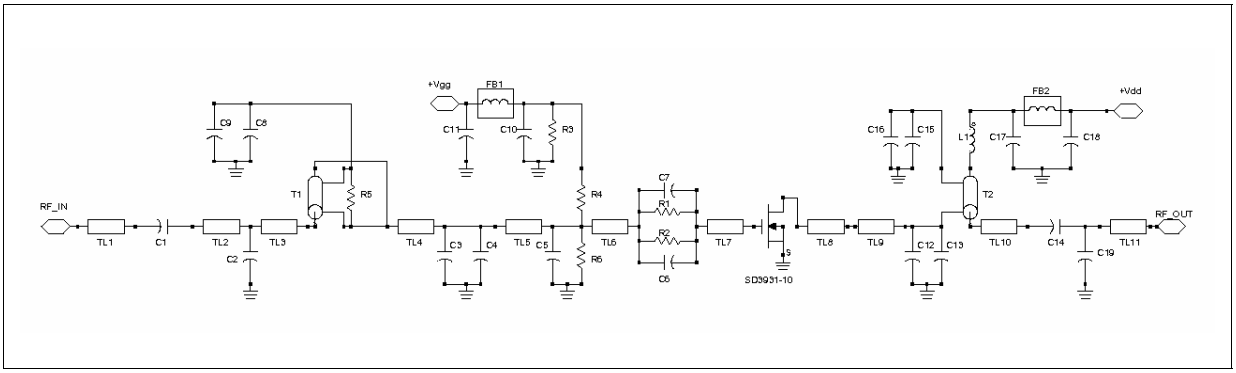


Table 8. Bill of materials

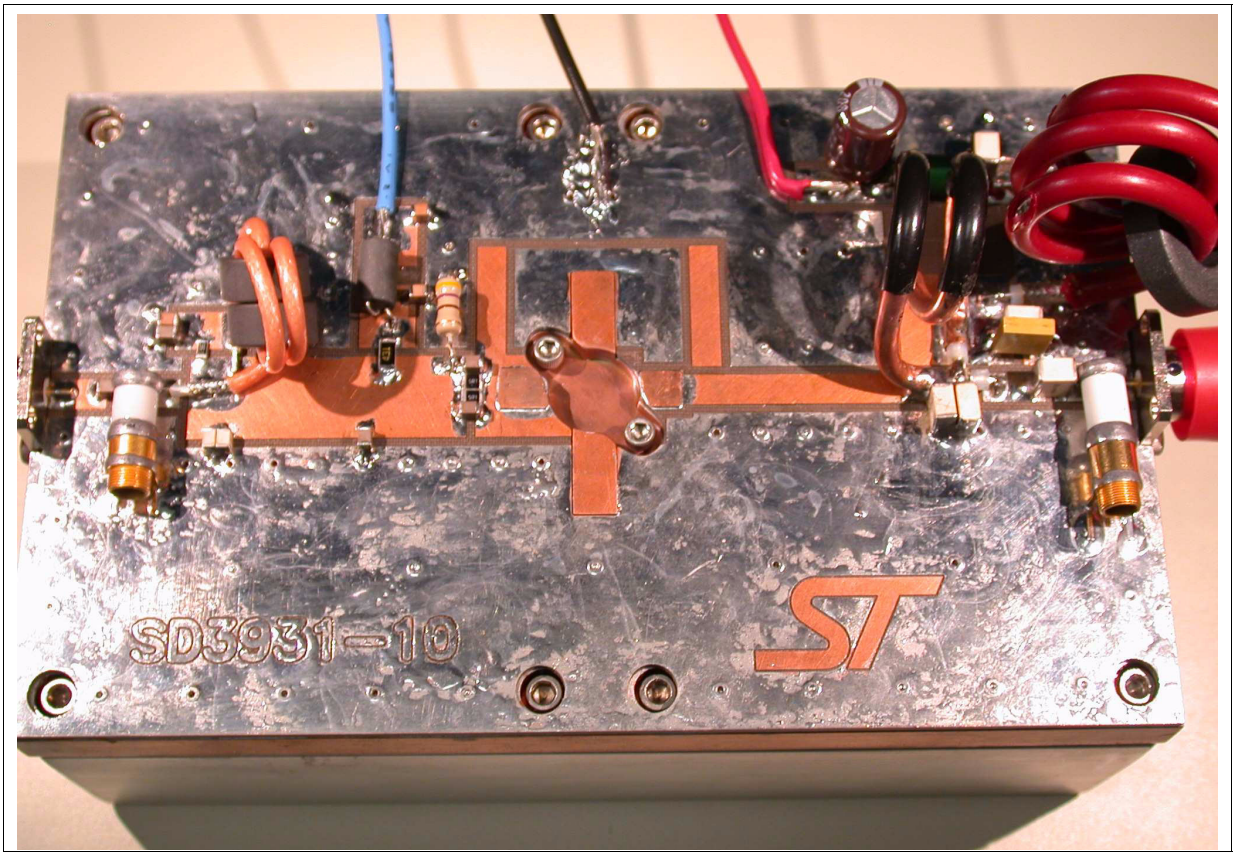
Component	Description
C1, C8	1200 pF ATC 700B chip capacitor
C2	1-20 Johanson air variable capacitor
C3, C4	120 pF ATC 100B chip capacitor
C5	300 pF ATC 100B chip capacitor
C6, C7	470 pF ATC 100B chip capacitor
C9, C10, C11	10,000 pF ATC 200B chip capacitor
C12, C16	470 pF ATC 100C chip capacitor
C13	120 pF ATC 100C chip capacitor
C14, C17	1,000 pF ATC 100C chip capacitor
C15	0.1 uF molded ceramic capacitor
C18	10 uF, 200 V electrolytic capacitor
C19	1-30 pF Johanson variable capacitor
R1, R2	5.1 Ω, 1/4 W chip resistor
R3	470 Ω, 1/8 W chip resistor
R4	430 Ω, 1/2 W chip resistor
R5	360 Ω, 1/8 W chip resistor
R6	470 ohm, 1/2 W carbon axial lead resistor
FB1, FB2	ferrite bead, VK200
L1	RG-141, 13.6" thru Fair-Rite toroid #2643801502, 3 turns
TI	4:1 transformer, 25 Ω coaxial cable, 6", thru 2 x Fair-Rite toroid # 5943001101, 2 turns
T2	1:4 transformer, 25 ohm semi-rigid coaxial cable, OD .141", 6", 2 turns
TL1	0.340" x 0.175" microstrip

Table 8. Bill of materials (continued)

Component	Description
TL2	0.135" x 0.175" microstrip
TL3	0.225" x 0.175" microstrip
TL4	0.175" x 0.500" microstrip
TL5	0.805" x 0.500" microstrip
TL6	0.600" x 0.500" microstrip
TL7	0.420" x 0.500" microstrip
TL8	0.265" x 0.240" microstrip
TL9	1.550" x 0.180" microstrip
TL10	0.360" x 0.175" microstrip
TL11	0.300" x 0.175" microstrip
PCB	0.062" woven glass, copper clad, Er = 2.55

6 Circuit layout

Figure 8. Circuit layout photo



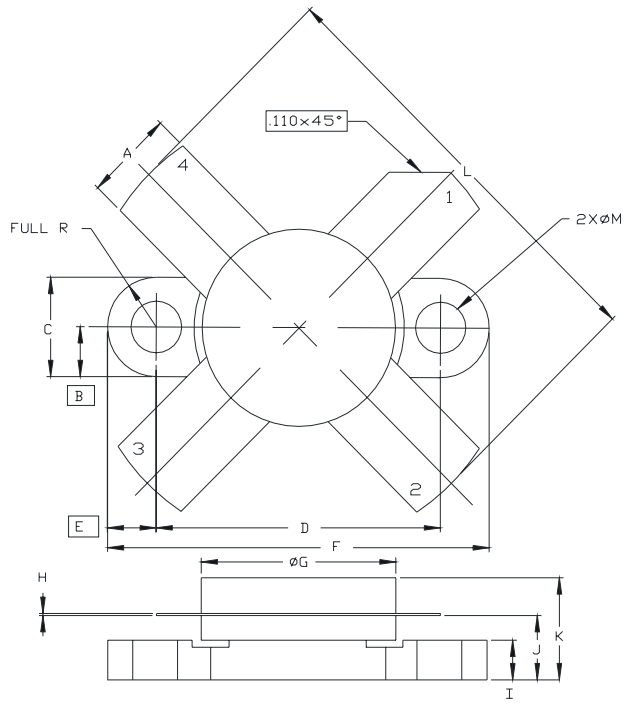
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 9. M174 (0.500 DIA 4/L N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.56		5.584	0.219		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.11		3.00	0.083		0.118
J	3.81		4.45	0.150		0.175
K			7.11			0.280
L	25.53		26.67	1.005		1.050
M	3.05		3.30	0.120		0.130

Figure 9. Package dimensions



Controlling Dimension: Inches

1011000D

8 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Jun-2007	1	First release
11-Jul-2007	2	Inserted *Table 7: Vgs sort (@250 mA) on page 7*
26-Oct-2007	3	Updated *Table 4: Static (per side) on page 4* Added *Section 5: Test circuit on page 8*, *Section 6: Circuit layout on page 9*
11-Jul-2008	4	Updated *Table 4: Static (per side) on page 4*

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